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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	19

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,003	KIRSCH, GRAHAM	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/13/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19-41,43-49 and 51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-10,14-17,19-21,28-31 and 36-39* is/are allowed.

6)☒ Claim(s) *1-6,11-13,22-27,33-35,41,43-49 and 51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1 – 6, 11 – 13, 22, 24 – 27, 33, and 35 are rejected under 35 U.S.C. 102(a) as being anticipated by Cambridge Parallel Processing (Gamma II Plus Technical Overview, hereinafter "CPP").

3. With respect to claims 1 – 2 and 22, CPP discloses a processing system comprising:

a processing unit (figure 2.1 on page 2-2, Microprocessor Controller); and

an active memory device coupled to said processing unit comprising:

a main memory (page 2-2, figure 2.1, Array Memory);

a plurality of processing elements (figure 2.1, PEs), each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection (page 2-10, PE Memory Size); and

a circuit coupled between said main memory and said plurality of processing elements (figures 2.1, 2.6 and pages 2-11 – 2-14, MCU) said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements, wherein said circuit is further adapted to write data from said plurality of processing elements to

said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (2-13, Array Interface, 2-10, Data Representation, 2-11, Array Memory Addresses).

4. With respect to claim 3 – 4 and 24 – 25, a plurality of processing elements in a first group are coupled to a plurality of data buses of said main memory, each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory (figure 2.1 and 2-10, PE Memory Size, each PE is directly connected to its own section of the array memory through a single bit data bus) wherein the first group includes eight processing elements (first row of the PE array in figure 2.1 includes 8 processing elements).

5. With respect to claim 5, CPP discloses an active memory device comprising:

a main memory (page 2-2, figure 2.1, Array Memory);

a plurality of processing elements (figures 2.1 and 2.2, Adder in a 1-bit processor in a PE array), each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection (page 2-10, PE Memory Size); and

a circuit (figure 2.2, an array of circuit elements surrounding the Adder) coupled between said main memory and said plurality of processing elements said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements (2-10, Data Representation), , wherein said circuit further comprises:

a plurality of circuits (figure 2.2, circuit elements surrounding the Adder), each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory (see figure 2.2).

6. With respect to claim 26, CPP discloses a processing system comprising:

a processing unit (figure 2.1 on page 2-2, Microprocessor Controller); and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory (page 2-2, figure 2.1, Array Memory);

a plurality of processing elements (figures 2.1 and 2.2, Adder in a 1-bit processor in a PE array), each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection, wherein a plurality of processing elements in a first group are coupled to a plurality of data buses of said main memory, each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory; and

a circuit coupled between said main memory and said plurality of processing elements (figure 2.2, an array of circuit elements surrounding the Adder), said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements (2-10, Data Representation, 2-11 Array Memory Addresses), wherein said circuit further comprises:

a plurality of circuits (figure 2-2, circuit elements surrounding the Adder of a 1-bit processor in a PE), each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory (page 2-10, Array Memory, PE Memory size).

7. With respect to claims 6 and 27, each of said plurality of circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to a respective one of a plurality of data buses (figure 2.2 S and D are coupled to the data bus, or array memory pin, which are in turn coupled to the input of the second multiplexer), each of said plurality of data buses being coupled to said main memory; and

a first multiplexer (figure 2.2, the 2nd multiplexor on the right hand side of the figure) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits (some are directly coupled and others are coupled through the 1st multiplexor and the adder), and an output coupled to its associated respective one of said plurality of processing elements (coupled through the 1st multiplexor on the left hand side of the figure).

8. With respect to claims 11 – 12 and 33, CPP discloses processing system comprising:

a processing unit (figure 2.1); and

a memory device coupled to said processing unit, said memory device comprising (figure 2.1, PE array and Array Memory);

a main memory (Array Memory);

a plurality of processing elements (figure 2.2, Adders), each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit and a single bit data input; and

a plurality of data path circuits (figure 2.2, array of circuit elements surrounding the Adder), each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements (2^{nd} Multiplexor input), at least a second input of said plurality being coupled to a respective one of a plurality of data buses of said main memory (1^{st} Multiplexor input from Array memory pin through S register), and an output coupled to said single bit input (1^{st} Multiplexor output) of a respective one of said plurality of processing elements,

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time, wherein each of said data path circuits is further adapted to write data from said plurality of processing elements to said main memory in a vertical mode and read data stored in

said main memory in a vertical mode from said main memory to said plurality of processing elements (2-13, Array Interface, 2-10, Data Representation).

9. With respect to claims 13 and 35, each of said plurality of data path circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit; and

a first multiplexer (2nd Multiplexor on the right hand side) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits (each of the inputs are either directly coupled to the logic circuits or indirectly coupled through the Adder), and an output coupled to said output of said data path circuit (there are two coupled outputs from this Multiplexor).

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 32, 40 – 41, 43, 44, 46 – 49 and 51 rejected under 35 U.S.C. 102(b) as being anticipated by Fung et al. (US Patent No. 4,380,046, hereinafter "Fung").

12. With respect to claims 32 and 40, Fung discloses a processing system comprising:

a processing unit (figure 1, 26); and

a memory device coupled to said processing unit (figure 1, 22), said memory device comprising:

a main memory (Claim 7, array of subunit C, claim 8, array of subunits D, also see figure 2, 50 for individual elements of this array that corresponds to an associated processing element) ;

a plurality of processing elements (claims 7, 8, NxM array of subunit A, also see figure 2, 54), each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input (figure 2); and

a plurality of data path circuits (claim 7, NxM array of subunit B, also see figure 2, 56, and figure 5), each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs (figure 5), a first input (one of the two inputs to 82) of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements (coupled to 52), at least a second input (input to the AND gate on the left of 82) of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory (coupled to 52), and an output (output of the tristate device 78) coupled to said single bit input of a respective one of said plurality of processing elements (coupled to 52),

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main

memory in a horizontal mode (see figures 2 and 3, memory elements of LMU is organized horizontally, also I/O through S registers of subunit C is done horizontally), and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time,

wherein each of said data path circuits is further adapted to write data from said plurality of processing elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (abstract, bits can be written in horizontal or vertical directions),

wherein said processing unit and said memory device are on a same chip (col. 5, lines 41 – 44).

13. With respect to claim 41, Fung discloses a method for writing data from a processing element to a memory device comprising the steps of:

providing a plurality of data bits in a serial manner (claim 7) from said processing element (NxM array of subunit A) to a data circuit (NxM array of subunit B);

passing said data through said data circuit; and

writing said data to said memory device (NxM array of subunit C) , wherein said data circuit passes said data directly to said memory device in a horizontal mode (abstract and claim 7, can move and store data in horizontal or vertical direction), wherein said step of passing the data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data bus (figure 4, each bit of the plurality of data bits are outputted on L1 or L2 lines of their respective subunit As as they travel across each node) associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address (as the bits move across the nodes their location in the memory device are associated with a different address, for example a bit moved from address (i, j-1) to (i,j) changes is now located in the memory device associate with address (i,j)).

14. With respect to claim 43, the step of outputting further comprises:

passing each bit of said plurality of data bits through a respective register (figure 5, 76).

15. With respect to claim 44, each different memory address has an associated plurality of bits (figure 2, 50 and 54), and wherein said step of writing each said data bit further comprises:

writing said each bit into a same bit of said associated plurality of bits in each said different memory address (abstract and claim 7, as data bits get written, or shifted to neighboring elements, each bit get written into a same bit in different memory address.)

16. With respect to claim 46 the step of passing said at least a portion of said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data line of a single data bus associated with said memory device (figure 5, 98, single data bus consists of four different lines tied together on which a data bit is output); and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to successive bit locations associated with a single address (figure 2, 54, and claim 3, BC/SR stores bits in successive locations.)

17. With respect to claim 47, the step outputting further comprises:

passing each bit of said plurality of data bits through a respective register (figure 2, 54, also see figure 6.)

19. With respect to claim 48, Fung discloses a method for reading data stored in a memory device and providing said data to a processing element, said method comprising the steps of:

providing a plurality of data bits from said memory device to a data circuit;

passing said data through said data circuit; and

outputting said data to said processing element in a serial manner (claim 7),

wherein at least a portion of data is store in said memory device in a vertical mode (abstract, data is moved and stored in horizontal or vertical directions).

19. With respect to claim 49, the step of passing said data further comprises:

passing each bit of data associated with a single address through a respective register (figure 5, 76); and

inputting said each bit of data associated with said single address to a multiplexer (80),

wherein said multiplexer outputs said each bit of data in a serial manner to said processing element (claim 7.)

20. With respect to claim 51, the step of passing said at least a portion of said data further comprises:

passing a respective bit of data associated with a different address through a respective register (figure 4, and figure 5, 76); and

inputting each said respective bit of data associated with said different address to a multiplexer (94),

wherein said multiplexer outputs said each said respective bit of data in a serial manner to said processing element (figure 5, 94, the multiplexer outputs bit of data to the processing element through coupling circuits.)

Allowable Subject Matter

21. Claims 7 – 10, 14 – 17, 19 – 21, 28 – 31 and 36 – 39 are allowed.

Response to Arguments

22. Applicant's arguments filed on 13 April 2004 have been fully considered but they are not persuasive.

23. With respect to independent claims 1, 11, 22 and 33, Applicant's argument regarding the CPP reference is not persuasive. The processor array may be directly coupled to the array memory as Applicant argued, but this does not preclude the MCU from being coupled between the PE's and the memory array. Figure 2.6 clearly shows that the MCU is coupled to the data array through its Array Support Unit. It is also coupled to the PEs via the Array Interface. Therefore, there is at least one path through which the MCU is coupled between the PEs and the memory array.

As to Applicant's argument that there is no data connection between the main memory and the PEs through the array interface and array support unit, the claims do not require that the data from the memory array to the processing elements ***pass through*** the circuit. They merely require that readings and writings be done by the circuit. MCU controls the overall operation of the processor/memory array including reading and writing to/from the memory array.

24. With respect to Applicant's argument against the Fung reference, Applicant's main arguments are that Fung's invention lacks "main memory" and that no data conversion is needed. As currently claimed, the "main memory" does not have any feature that is patentably distinct from any other memory that a system may use to store and process data. As to the data conversion argument, this is not a claimed feature of the claimed circuit. Fung's circuit enables the processing elements, which collectively include a "main memory", to read and write vertically and horizontally from the neighboring elements.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nickolls et al. (US Patent No. 5,243,699) and Kahle et al. (US Patent No. 5,148,547) disclose bit serial processor array systems with data conversion circuits. Wilson (US Patent No. 5,557,734), Bromley (US Patent No. 5,247,613), Jackson et al. (US Patent No. 5,157,785) and Li (US Patent No. 5,038,386) disclose other bit serial processors based parallel computing systems that transpose data.

26. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
whc
June 29, 2004

MATTHEW KIM
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